SET-A

IOPS Quiz-1

B.Tech. (ECE) – 3rd Semester; Session: July-Dec. 2018

Full Marks: 60, TIME: 60 Minutes

Course Instructor: Dr. S. MAITY (I.T.)

Choose the most appropriate answers. **Correct Answer = 1 Mark; Incorrect Answer = -1 Mark.**

1. If address bus size is 12 bits and word size is 2 bytes, how much main memory (RAM) could be attached to the system?
   a. 8KB b. 10KB c. 4KB d. 6KB
2. CPU communicates with a peripheral I/O Device through:-
   a. Main Memory & system bus b. Device Controller & Main Memory
   c. System bus d. Device Controller & System bus
3. According to the decreasing order of access speed, by the CPU, which of the following order is correct?
   a. CPU Register -> CPU Cache -> Main Memory -> Secondary Storage
   b. Secondary Storage -> Main Memory -> CPU Cache -> CPU Register
   c. CPU Cache -> CPU Register -> Main Memory -> Secondary Storage
   d. Main Memory -> Secondary Storage -> CPU Cache -> CPU Register
4. Which of the following represents an incorrect hierarchy?
   a. H/W -> Kernel -> System Program -> Application Program
   b. Users -> Application Program -> O/S -> H/W
   c. H/W -> Application Program -> System Program -> Users
   d. Users -> Application Program -> Kernel -> H/W
5. Which of the following is not an essential part of an O/S Kernel?
   a. CPU Scheduling Program b. Antivirus Program
   c. Memory management Program d. Interprocess communication Program
6. Which of the following is not an essential part of a microkernel?
   a. Memory management Program b. Process management Program
   c. Interprocess communication Program d. Deadlock handling Program
7. Multitasking is a logical extension of multiprogramming with an essential criteria of:-
   a. Short average response time b. High throughput
   c. High CPU utilization d. Low memory requirement
8. Which of the following is known as a tightly coupled system?
   a. Multitasking system b. Multiprogramming system
   c. Multiprocessor system d. Distributed system
9. What is the relation between a distributed system and a computer network?
   a. They are synonymous to each other
   b. A Computer network is built on top a distributed system
   c. There is no such direct relation between the two
   d. A distributed system is built on top a Computer network
10. Which of the following are the two essential criteria for a real time system?
    a. Correctness and timeliness b. Efficiency and throughput
    c. Efficiency and user convenience d. Correctness and efficiency
11. A hard real time system is one where:-
    a. At least one of the process must finish before its deadline
    b. All of the processes must finish before their deadlines
    c. Most of the processes must finish before their deadlines
    d. All processes must finish before their deadline with a high probability
12. Which of the following could be considered as a soft real time application?
    a. Automatic missile launching application b. Automatic traffic signal controlling application
    c. Fibonacci Series printing application d. Multimedia data transmission application
13. Device controller is an example of:-
    a. Microprocessor b. Microcontroller
    c. Embedded system d. General purpose computer system
14. Bootstrap Program is permanently stored in:-
    a. RAM b. ROM c. Swap space d. CPU Cache

SET-A

15. What is a ‘trap’?
    a. A special system call
    b. A H/W interrupt generated due to error
    c. A S/W interrupt generated due to error
    d. A H/W or S/W interrupt generated due to error
16. Where interrupt vector is kept by O/S?
    a. At ROM
    b. At a fixed location in RAM
    c. Any available location in RAM
    d. Swap space of the secondary storage
17. A computer system has a 32-bits address Bus and it can handle a total of 256 types of interrupts (h/w and s/w). Then what is the size of the Interrupt Vector?
    a. 2^{10} bytes b. 256 x 5 bytes c. 256 bytes d. 4 bytes
18. How a CPU instructs an I/O device controller?
    a. By setting proper values in memory controller
    b. By sending an interrupt signal to the device controller
    c. By setting proper values in instruction register
    d. By setting proper values in device controller registers
19. How an I/O device controller informs to the CPU about the completion of some I/O operation?
    a. By sending an interrupt signal to CPU
    b. By setting proper values in CPU register
    c. By setting proper values in device controller registers
    d. By sending an interrupt signal to the I/O device
20. A process may go to the ‘waiting’ state from the ‘running’ state:-
    a. In case of a synchronous I/O
    b. In case of an asynchronous I/O
    c. In both of the above two cases
    d. None of the above cases
21. Multiple I/Os can execute concurrently in:-
    a. Synchronous I/O
    b. Asynchronous I/O
    c. Both (a) and (b)
    d. None of the above
22. Suppose a process P requested for some I/O. When the I/O is complete, process Q is already running in CPU. Now process P is in which of the following states?
    a. Running state b. Ready state c. Waiting state d. Terminated state
23. Device status table maintain information for all the processes in the system which are currently in:-
    a. Running state b. Ready state c. Waiting state d. Terminated state
24. Which of the following state transition is not possible?
    a. Ready to running
    b. Running to ready
    c. Running to waiting
    d. Ready to waiting
25. Which of the following could be a valid cause of a transaction of state from ‘waiting’ to ‘ready’ for a process P?
    a. Process P requested for an I/O
    b. A child process of the process P terminated
    c. CPU received a timer interrupt
    d. A new process Q is admitted into the system
26. A Program of the O/S which takes the control of the CPU from One process P, and gives it to another process Q is known as:-
    a. Scheduler
    b. Dispatcher
    c. Interpreter
    d. Compiler
27. A PCB for a process P is stored at which location?
    a. O/S address space
    b. Code segment of process P’s address space
    c. Data segment of process P’s address space
    d. Stack segment of process P’s address space
28. Which of the following is a possible advantage that could be obtained by using DMA (Direct Memory Access)?
    a. Increased data transfer speed from a low speed I/O device
    b. Increased data transfer speed from a low speed I/O memory
    c. Reduced number of interrupts received by CPU
    d. Reduced volume of data transferred from an I/O device controller
29. Which of the following units of a computer system is not an ‘active’ device, i.e., cannot execute instructions?
    a. CPU b. Device Controller c. DMA Controller d. I/O Device
30. Following are some pairs of computer H/W units. In which pairs, the execution of one unit can slow down the execution of the other?
    a. CPU and a DMA Controller
    b. CPU and a Device Controller

c. Device Controller and another Device controller d. None of the above

31. Which phenomenon is known as 'Cycle stealing DMA'?
    a. CPU and DMA Controller competing for CPU cycles
    b. CPU and DMA Controller competing for DMA cycles
    c. CPU and DMA Controller competing for Memory cycles
    d. CPU and DMA Controller competing for I/O cycles
32. What happens if a privileged instruction is incorporated in a user program?
    a. It generates a trap b. It switches the 'mode bit' to privilege mode
    c. It switches the 'mode bit' to user mode d. It invokes a system call
33. What is dual mode of operation in O/S?
    a. User mode and sleep mode b. System mode and privilege mode
    c. Privilege mode and supervisor mode d. User mode and monitor mode
34. System calls are interface between:-
    a. Application program and system program b. Application program and kernel
    c. Application program and H/W d. Kernel and H/W
35. Who implements the body of a system call function?
    a. O/S Kernel b. A Programming Language Library
    c. A Programming Language Compiler d. System Programs
36. How many different approaches are there for passing parameters (arguments) to a system call?
    a. 1 b. 2 c. 3 d. 4
37. By O/S Literature, System Calls are usually classified in how many different categories?
    a. 2 b. 3 c. 4 d. 5
38. An O/S with microkernel:-
    a. Runs all process in privilege mode b. Runs essential O/S processes in user mode
    c. Runs all processes in user mode d. Runs non-essential O/S processes in user mode
39. Communication between an user process and a file server in a microkernel O/S is an example of:-
    a. Message passing communication b. Shared memory communication
    c. RPC d. All of the above
40. Communication between an user process and a file server in a microkernel O/S is an example of:-
    a. Message passing communication b. Client-Server communication
    c. Indirect communication d. All of the above
41. Which of the following cannot be an advantage of using microkernel?
    a. Computation speedup b. Compatibility with small size RAM
    c. Ease of O/S update without restarting the system d. Increased security and reliability
42. Usually a microkernel is prescribed for use in:-
    a. Real time Systems b. Embedded Systems
    c. Client-Server Systems d. General purpose computer systems.
43. Virtual machine implementation S/W can run only in:-
    a. Physical monitor mode b. Virtual user mode
    c. Physical user mode d. Virtual monitor mode
44. An application program in a virtual machine can run only in:-
    a. Physical monitor mode b. Virtual monitor mode
    c. Virtual user mode d. All of the above
45. How resource partitioning is implemented in the virtual machine concept?
    a. Implemented by the virtual machine implementation S/W
    b. Implemented by the virtual machine kernels
    c. Resources are partitioned by the users
    d. Resources are partitioned by a system administrator
46. Which of the following cannot be an advantage of using multiple virtual machines for multiple users in a physical machine?
    a. Better security and protection b. Ease of O/S development for research purpose
    c. Better utilization of H/W resources d. None of the above
47. If a privileged instruction is executed at a virtual machine kernel, it would:-
    a. Generate a trap (H/W interrupt to CPU)
    b. Modify the content of some device controller
    c. Sends an erroneous value to the server

SET-A

d. Invoke privileged instructions in virtual machine implementation S/W

48. A process currently residing in main memory might be in which of the following states?
    a. Ready, Waiting or Running b. Ready or Running
    c. Ready or Waiting d. New, Ready or Waiting
49. Which of the following scheduling algorithms is supposed to take optimal decisions?
    a. Short-term scheduler b. Long-term scheduler
    c. Medium-term scheduler d. All of the above
50. Degree of multiprogramming could be adjusted by:-
    a. Short-term scheduler b. Long-term scheduler
    c. Medium-term scheduler d. All of the above
51. An O/S not allocating any swap space, cannot contain:-
    a. A Short-term scheduler b. A Long-term scheduler
    c. A Medium-term scheduler d. None of the above
52. Which of the following factor has no direct effect on dispatch latency? (Context switch time)
    a. Optimality of long-term scheduler b. Size of the swap space available
    c. Main memory speed d. Complexity of the O/S
53. Suppose the 'send' and 'receive' primitives are implemented as: *send*(P,msg), *receive*(id,msg); where P is a process-id, msg is a pointer to message structure, and id is a pointer to a process-id. What type of communication it implements?
    a. Symmetric indirect b. Symmetric direct c. Asymmetric direct d. Asymmetric indirect
54. Which of the following is not correct for an indirect communication?
    a. Links between processes are not preexisting
    b. One and only one Link could be established between any two process
    c. More than two process can be attached to the same Link
    d. None of the above
55. In which of the following cases, send primitive must be blocking?
    a. Asynchronous communication b. Bounded capacity buffering
    c. Unbounded capacity buffering d. Zero capacity buffering
56. A socket is a combination of:-
    a. Source IP Address and destination IP Address b. IP Address and Port number
    c. Source Port number and destination Port number d. All of the above
57. What could be a port number for a client socket?
    a. Any integer b. Any integer below 1024
    c. Any integer above 1024 d. Only some specific predefined integers
58. What could be transmitted between two sockets?
    a. Formatted message b. Unformatted bit stream c. Both d. None
59. RPC is built on top of:-
    a. Message passing communication system b. Shared memory communication system
    c. Peer to peer communication system d. Broadcast communication system
60. An RPC 'stub' is incorporated/executed at:-
    a. Client side b. Server side c. Both side d. No where

SET-A

ANSWER SHEET

NAME:_____ Enroll. No.

_____

TICK (√) ON THE CORRECT CELLS (Finalize your answer and then only tick. If there is any confusion on which option you have ticked, TAs have full right to cancel the answer/give negative marks):-

Q. No.	A	B	C	D		Q. No.	A	B	C	D
1	√					31			√	
2				√		32	√			
3	√					33				√
4			√			34		√		
5		√				35	√			
6				√		36			√	
7	√					37				√
8			√			38				√
9				√		39	√			
10	√					40				√
11		√				41	√			
12				√		42		√		
13			√			43	√			
14		√				44			√	
15				√		45	√			
16		√				46			√	
17	√					47				√
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19	√					49		√		
20			√			50		√		
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26		√				56		√		
27	√					57			√	
28			√			58		√		
29				√		59	√			
30	√					60			√	